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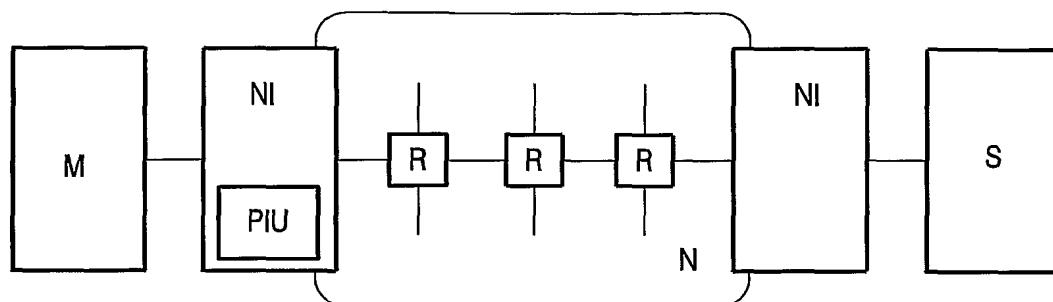
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(54) Title: INTEGRATED CIRCUIT AND METHOD FOR PACKET SWITCHING CONTROL



(57) Abstract: An integrated circuit having a plurality of processing modules (M, S) and an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a packet based communication based on transactions between said plurality of processing modules (M, S) is provided. Each packet comprises a first predetermined number of subsequent words each having a second predetermined number of bits. A first of said plurality of processing modules (M) issues a transaction by sending at least one packet over said interconnect means (N) to a second of said plurality of processing modules (S). The integrated circuit further comprises at least one packet inspecting unit (PIU) for inspecting bits of said at least one packet to determine bits not required for said issued transaction and for matching said not required bits of said at least one inspected packet with other bits of the same packet.

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